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NTE74HC595
NTE74HC595T
Integrated Circuit
TTL – High Speed CMOS,
8–Bit Serial–In or Parallel–Out Shift Register w/3–State Outputs

Description:

The NTE74HC595 (16–Lead DIP) and NTE74HC595T (SOIC–16) are 8–stage serial shift registers with storage register and 3–state outputs. The registers have separate clocks. These high–speed Si–gate CMOS devices and are pin compatible with Low–power Schottky TTL (LSTTL).

Data is shifted on the positive–going transitions of the shift register clock input (SHCP). The data in each register is transferred to the storage register on a positive–going transition of the storage register clock input (STCP). If both clocks are connected together, th shift register will always be one lock pulse ahead of the storage register.

The shift register has a serial input (DS) and a serial standard output (Q7S) for cascading. It is also provided with asynchronous reset (active LOW) for all 8 shift register stages. The storage register has 8 parallel 3–state bus driver outputs. Data in the storage register appears at the output whenever the output enable input ($\overline{OE}$) is LOW.

Features:

- 8–Bit Serial Input
- 8–Bit Serial or Parallel Output
- Storage Register with 3–State Outputs
- Shift Register with Direct Clear
- 100Mhz (typical) Shift Out Frequency
- Negative–Edge Clocking

Applications:

- Serial–to–Parallel Data Conversion
- Remote Control Holding Register

Absolute Maximum Ratings: (Voltages referenced to GND (ground = 0V))

Supply Voltage, V_{CC} . . . . . –0.5 to +7.0V
Input Clamping Current ($V_I < -0.5V$ or $V_I > V_{CC} +0.5V$), I_{IK} . . . . . ±20mA
Output Clamping Current ($V_O < -0.5V$ or $V_O > V_{CC} +0.5V$), I_{OK} . . . . . ±20mA
Output Current ($V_O = -0.5V$ to ($V_{CC} +0.5V$)), I_O
  Pin Q7S . . . . . ±25mA
  Pins Qn . . . . . ±35mA
Supply Current, I_{CC} 70mA
Minimum Ground Current, I_{GND} . . . . . –70mA
Total Power Dissipation, P_{tot}
  NTE74HC595 . . . . . 750mW
    Derate Linearly Above +70°C 12mW/K
  NTE74HC595T 500mW
    Derate Linearly Above +70°C 8mW/K
Maximum Junction Temperature Range, T_J . . . . . –40°C to +125°C
Storage Temperature Range, T_{stg} . . . . . –65°C to +150°C

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.0	5.0	6.0	V
Input Voltage	V_I	0	–	V_{CC}	V
Output Voltage	V_O	0	–	V_{CC}	V
Input Transition Rise and Fall Rate	±t/±V				
V_{CC} = 2.0V		–	–	625	ns/V
V_{CC} = 4.5V		–	1.67	139	ns/V
V_{CC} = 6.0V		–	83	–	ns/V
Ambient Temperature Range	T_A	–40	+25	+125	°C

Static Characteristics: (At recommended operating conditions; voltages are referenced to GND (ground = 0V))

Parameter	Symbol	Test Conditions		–40° to +85°C			–40° to +125°C		Unit
				Min	Typ	Max	Min	Max	
HIGH Level Input Voltage	V_{IH}	V_{CC} = 2.0V		1.5	1.2	–	1.5	–	V
		V_{CC} = 4.5V		3.15	2.4	–	3.15	–	V
		V_{CC} = 6.0V		4.2	3.2	–	4.2	–	V
LOW Level Input Voltage	V_{IL}	V_{CC} = 2.0V		–	0.8	0.5	–	0.5	V
		V_{CC} = 4.5V		–	2.1	1.35	–	1.35	V
		V_{CC} = 6.0V		–	2.8	1.8	–	1.8	V
HIGH Level Output Voltage All Outputs	V_{OH}	V_I = V_{IH} or V_{IL}, I_O = –20↑A	V_{CC} = 2.0V	1.9	2.0	–	1.9	–	V
			V_{CC} = 4.5V	4.4	4.5	–	4.4	–	V
			V_{CC} = 6.0V	5.9	6.0	–	5.9	–	V
Q7S Output		V_I = V_{IH} or V_{IL}	I_O = –4mA, V_{CC} = 4.5V	3.84	4.32	–	3.7	–	V
			I_O = –5.2mA, V_{CC} = 6.0V	5.34	5.81	–	5.2	–	V
Qn Bus Driver Outputs		V_I = V_{IH} or V_{IL}	I_O = –6mA, V_{CC} = 4.5V	3.84	4.32	–	3.7	–	V
			I_O = –7.8mA, V_{CC} = 6.0V	5.34	5.81	–	5.2	–	V
LOW Level Output Voltage All Outputs	V_{OL}	V_I = V_{IH} or V_{IL}, I_O = 20↑A	V_{CC} = 2.0V	–	0	0.1	–	0.1	V
			V_{CC} = 4.5V	–	0	0.1	–	0.1	V
			V_{CC} = 6.0V	–	0	0.1	–	0.1	V
Q7S Output		V_I = V_{IH} or V_{IL}	I_O = 4mA, V_{CC} = 4.5V	–	0.15	0.33	–	0.4	V
			I_O = 5.2mA, V_{CC} = 6.0V	–	0.16	0.33	–	0.4	V
Qn Bus Driver Outputs		V_I = V_{IH} or V_{IL}	I_O = 6mA, V_{CC} = 4.5V	–	0.15	0.33	–	0.4	V
			I_O = 7.8mA, V_{CC} = 6.0V	–	0.16	0.33	–	0.4	V
Input Leakage Current	I_I	V_I = V_{CC} or GND, V_{CC} = 6.0V		–	–	±1.0	–	±1.0	↑A
OFF–State Output Current	I_{OZ}	V_I = V_{IH} or V_{IL}, V_{CC} = 6.0V, V_O = V_{CC} or GND		–	–	±5.0	–	±10	↑A
Supply Current	I_{CC}	V_I = V_{CC} or GND, I_O = 0A, V_{CC} = 6.0V		–	–	80	–	160	↑A
Input capacitance	C_I			–	3.5	–	–	–	pF

Dynamic Characteristics: (Voltages are referenced to GND (ground = 0V))

Parameter	Symbol	Test Conditions		+25°C (Note 1)			−40° to +85°C		−40° to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
Propagation Delay SHCP to Q7S	t_{pd}	Note 2	V_{CC} = 2.0V	–	50	160	–	200	–	240	ns
			V_{CC} = 4.5V	–	19	32	–	40	–	48	ns
			V_{CC} = 6.0V	–	15	27	–	34	–	41	ns
STCP to Qn		Note 2	V_{CC} = 2.0V	–	55	175	–	220	–	265	ns
			V_{CC} = 4.5V	–	20	35	–	44	–	53	ns
			V_{CC} = 6.0V	–	16	30	–	37	–	45	ns
$\overline{MR}$ to Q7S		Note 3	V_{CC} = 2.0V	–	47	175	–	220	–	265	ns
			V_{CC} = 4.5V	–	17	35	–	44	–	53	ns
			V_{CC} = 6.0V	–	14	30	–	37	–	45	ns
Enable Time $\overline{OE}$ to Qn	t_{en}	Note 4	V_{CC} = 2.0V	–	47	150	–	190	–	225	ns
			V_{CC} = 4.5V	–	17	30	–	38	–	45	ns
			V_{CC} = 6.0V	–	14	26	–	33	–	38	ns
Disable Time $\overline{OE}$ to Qn	t_{en}	Note 5	V_{CC} = 2.0V	–	41	150	–	190	–	225	ns
			V_{CC} = 4.5V	–	15	30	–	38	–	45	ns
			V_{CC} = 6.0V	–	12	27	–	33	–	38	ns
Pulse Width SHCP HIGH or LOW	t_w	V_{CC} = 2.0V		75	17	–	95	–	110	–	ns
		V_{CC} = 4.5V		15	6	–	19	–	22	–	ns
		V_{CC} = 6.0V		13	5	–	16	–	19	–	ns
STCP HIGH or LOW		V_{CC} = 2.0V		75	11	–	95	–	110	–	ns
		V_{CC} = 4.5V		15	4	–	19	–	22	–	ns
		V_{CC} = 6.0V		13	3	–	16	–	19	–	ns
$\overline{MR}$ LOW		V_{CC} = 2.0V		75	17	–	95	–	110	–	ns
		V_{CC} = 4.5V		15	6	–	19	–	22	–	ns
		V_{CC} = 6.0V		13	5	–	16	–	19	–	ns
Set−Up Time DS to SHCP	t_{su}	V_{CC} = 2.0V		50	11	–	65	–	75	–	ns
		V_{CC} = 4.5V		10	4	–	13	–	15	–	ns
		V_{CC} = 6.0V		9	3	–	11	–	13	–	ns
SHCP to STCP		V_{CC} = 2.0V		75	22	–	95	–	110	–	ns
		V_{CC} = 4.5V		15	8	–	19	–	22	–	ns
		V_{CC} = 6.0V		13	7	–	16	–	19	–	ns
Hold Time DS to SHCP	t_h	V_{CC} = 2.0V		3	−6	–	3	–	3	–	ns
		V_{CC} = 4.5V		3	−2	–	3	–	3	–	ns
		V_{CC} = 6.0V		3	−2	–	3	–	3	–	ns

Note 1. Typical values are measured at nominal supply voltage.
Note 2. t_{pd} is the same as t_{PHL} and t_{PLH}.
Note 3. t_{pd} is the same as t_{PHL} only.
Note 4. t_{en} is the same as t_{PZL} and t_{PZH}.
Note 5. t_{dis} is the same as t_{PLZ} and t_{PHZ}.

Dynamic Characteristics: (Voltages are referenced to GND (ground = 0V))

Parameter	Symbol	Test Conditions	+25°C (Note 1)			−40° to +85°C		−40° to +125°C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
Recovery Time $\overline{MR}$ to SHCP	t_{rec}	V_{CC} = 2.0V	50	−19	–	65	–	75	–	ns
		V_{CC} = 4.5V	10	−7	–	13	–	15	–	ns
		V_{CC} = 6.0V	9	−6	–	11	–	13	–	ns
Maximum Frequency SCHP to STCP	f_{max}	V_{CC} = 2.0V	9	30	–	4.8	–	4	–	MHz
		V_{CC} = 4.5V	30	91	–	24	–	20	–	MHz
		V_{CC} = 6.0V	35	108	–	28	–	24	–	MHz
Power Dissipation Capacitance	C_{PD}	f_i = 1Mhz, V_I = GND to V_{CC}, Note 6, Note 7	–	115	–	–	–	–	–	pF

Note 1. Typical values are measured at nominal supply voltage.

Note 6. C_{PD} is used to determine the dynamic power dissipation (P_D in ↑W).
$P_D = C_{PD} \times V_{CC}^2 \times f_i + ° (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in Mhz;
f_o = output frequency in Mhz;
$° (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V.

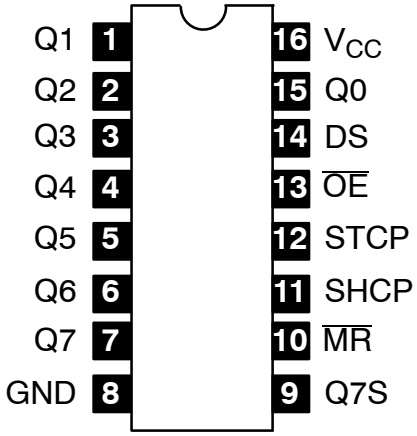
Note 7. All 9 outputs switching.

Functional Description:

Control				Input	Output		Function
SHCP	STCP	$\overline{OE}$	$\overline{MR}$	DS	Q7S	Qn	
X	X	L	L	X	L	NC	a LOW−level on $\overline{MR}$ only affects the shift registers
X	↑	L	L	X	L	L	empty shift register loaded into storage register
X	X	H	L	X	L	Z	shift register clear; parallel outputs in high−impedance OFF−state
↑	X	L	H	H	Q6S	NC	logic HIGH−level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q6S) appears on the serial output (Q7S).
X	↑	L	H	X	NC	QnS	contents of shift register stages (internal QnS) are transferred to the storage register and parallel output stages.
↑	↑	L	H	X	Q6S	QnS	contents of shift register shifted through; previous contents of the shift register is transferred to the storage register and th parallel output stages

H = HIGH voltage state;
L = LOW voltage state;
↑ = LOW−to−HIGH transition;
X = don't care;
NC = no change;
Z = high−impedance OFF−state

Pin Connection Diagram



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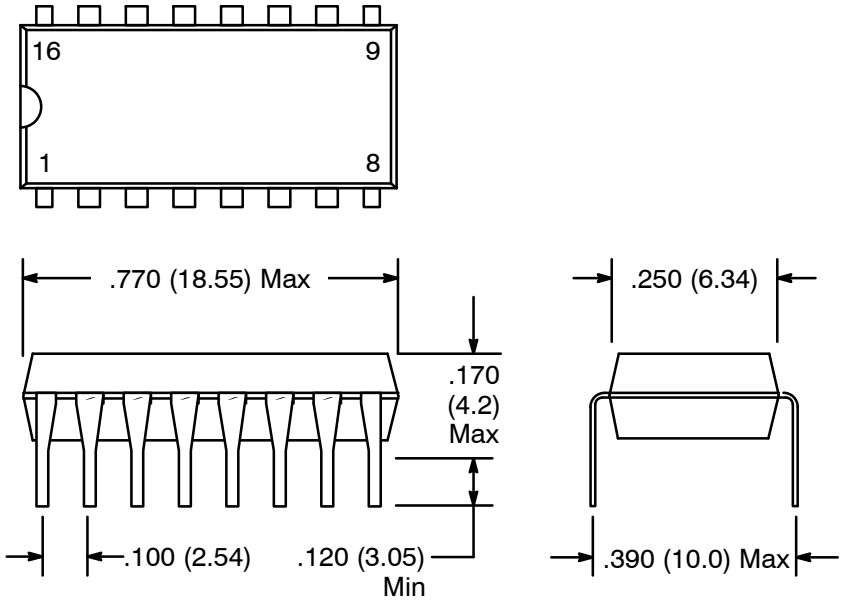

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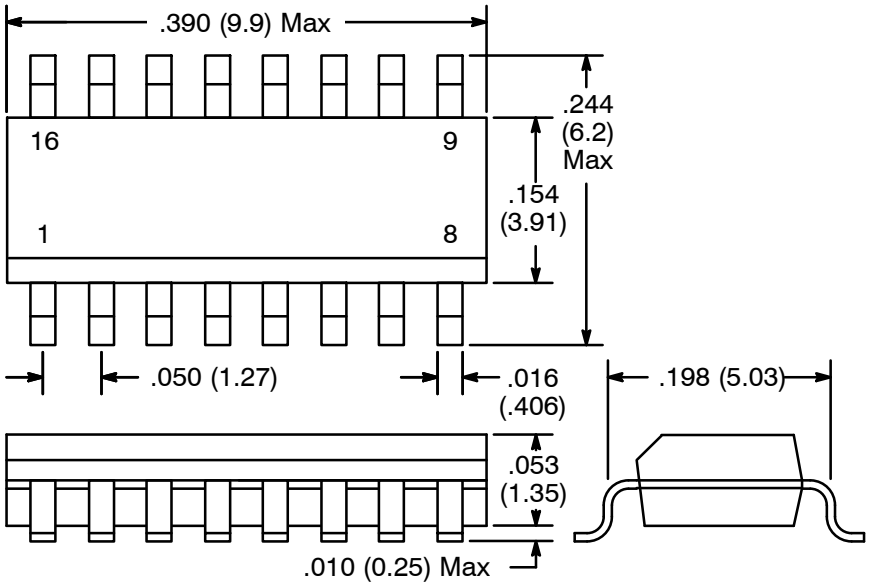

NOTE: Pin1 on Beveled Edge